Texas A&M
Semiconductor Institute

Advanced Packaging Co-Design/EDA Technical Symposium Agenda

Date: Friday September 27, 2024

Location: **Texas A&M-Fort Worth Campus**

Burnett Plaza, 2nd Floor

801 Cherry Street

Fort Worth, Texas 76102

8:30 AM – 9:00 AM: Registration and Breakfast

- **Registration Desk:** Attendees check-in, receive badges, and symposium materials.
- **Breakfast:** Light refreshments and networking opportunities.

9:00 AM – 9:15 AM: Welcome and Opening Remarks

- **Welcome Address:** Dr. Steve Putna, Director Texas A&M Semiconductor Institute
- **Opening Remarks:** Overview of the symposium objectives and schedule aligned to CHIPS Packaging Program Drivers:

9:15 AM - 10:00 AM: Keynote Address

- **Speaker:**
    - Albert Zeng, Sr Software Engineering Group Director, Cadence

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10:00 AM - 11:00 AM: Panel Session 1

- **Topic:** Leveraging AI to Accelerate Multi-Chiplet System Co-design and EDA Processes
- **Moderator:** Paul V. Gratz, Texas A&M
- **Panelists:**
    - Jiang Hu, Texas A&M

- Vidya Chhabria, ASU
- Andras Vass-Varnai, Siemens

11:00 AM – 11:20 AM: Break

- **Refreshments and Networking**

11:20 AM - 12:20 PM: Panel Session 2

- **Topic:** What's the role of EDA in the Security of Semiconductor Packaging?
- **Moderator:** JV Rajendran, Texas A&M
- **Panelists:**
  - Sudhir Mathane, AMD
  - Yiorgos Makris, UT Dallas
  - Jaimal M. Williamson, TI

12:20 PM - 1:30 PM: Buffet Lunch & Keynote Speaker

- **Speaker:** Oren Roades - Senior Director of R&D, Texas Instruments

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1:30 PM – 2:15 PM: Breakout Session 1

- Working Group 1: Management and Governance (Jiang Hu/Steve Putna /Arum Han - Session Chair)
- Working Group 2: EDA Co-Design for Advanced Packaging (Anastasia Muliana, Paul Gratz - Session Chair)
- Working Group 3: How should one use AI/ML in package design for test, repair, security, and reliability (Weiping Shi / Rainer Fink - Session Chair)

2:15 PM - 2:30 PM: Networking/Break

2:30 PM – 3:15 PM: Breakout Session 2

- Working Group 4: Co-design capabilities levering assembly substrate and processes comprehending power, thermal management and connector solutions (Anastasia Muliana, Jonathan Felts - Session Chair)

- Working Group 5: Prototype development in exemplar applications to speed yield/reliability advances (e.g. AI/low power) (Stavros Kalafatis, Paul Gratz - Session Chairs)
- Working Group 6: EDA-enabled incorporation and co-optimization of chiplets with high-speed electrical, photonic interconnect (Sam Palermo, Ajay Joshi)

3:15 PM - 3:30 PM: Networking/Break

3:30 PM – 4:15 PM: Breakout Session 3

- Working Group 7: EDA Standards, EDA interoperability; EDA-enabled incorporation and co-optimization (Jiang Hu - Session Chair)
- Working Group 8: Chiplet Security (JV Rajendran – Session Chair)
- Working Group 9: Education and WorkForce Development for Sustainable Semiconductor Ecosystem (Melia Jones/Akash Tyagi/Cindy Lawley - Session Chair)

4:15 PM - 5:00 PM: Individual Working Group Wrap-Up's & Closing Remarks

- Dr. Jeyavijayan Rajendran, Texas A&M Associate Professor, Electrical & Computer Engineering, ASCEND Fellow

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5:00PM: Adjourn followed by No-Host Networking (Optional)